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Inhomogeneous Bonding in Low-Temperature-Soldering: Brief Review

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Review

Thermal stresses [1-4] in solder joint interconnections (see, e.g., [5]) used in electronic and photonic packaging are proportional to the thermal contraction mismatch strains $\Delta\alpha\Delta T$ [3-9]. Here $\Delta\alpha$ is the effective coefficient of thermal expansion (CTE) mismatch between the soldered materials (the chip or the package to their substrates), and ΔT is the change in temperature from the elevated manufacturing (bonding/fabrication/soldering) temperature, at which, because of the interaction of shrinkage and stress-relaxation processes, the induced stresses are next-to-zero, to the low, room, testing or operation, temperature, at which the induced stresses are the highest. Clearly, these stresses are lower for lower soldering temperatures, and therefore there is an obvious incentive for using low temperature solders. What is less obvious is that significant stress relief in solder joints can be achieved also by employing, for the same materials and the same thermal mismatch strain $\Delta\alpha\Delta T$, inhomogeneous bonds [10-19], when, e.g., a solder material with a high soldering temperature and/or with a high Young's/shear modulus is employed in the mid-portion of the assembly, where the stresses in this material are low (at the mid-cross-section of the assembly these stresses, distributed in an anti-symmetric fashion, are always zero), and a low-melting-point solder and/or a solder with a lower modulus is employed at the assembly's peripheral portions, where the interfacial shearing and peeling thermal stresses are the highest. Ultimately, when only the elevated stresses, and not heat transfer considerations, are viewed to be critical, even assemblies bonded at the ends only are viable [16,17]. The incentive for the application of inhomogeneously soldered assemblies is due also to the attractive opportunity to use solders with high thermal conductivity in the assembly's major mid-portion (thereby having a design with good heat transfer properties at the location of the die) and employ solders, or even epoxies, at the assembly's relatively short peripheral portions, where the induced stresses are the highest and where the physical (mechanical) design considerations aimed at low thermal stresses are particularly critical. It has been shown particularly [18] that significant reduction in the level of the interfacial thermal stresses can be achieved, if one requires that these stresses (the shearing or the effective ones, when peeling is also considered) at the ends of an inhomogeneously bonded assembly are equal to the stresses at the boundaries between the assembly's long mid-portion, where high-modulus and/or high-melting-temperature solder is applied, and short peripheral portions, where a low-modulus and/or a low-melting-point solder (or even an epoxy adhesive) is used. Calculations indicate that each of the two maxima stresses, acting at the assembly ends and at the boundaries of its mid-portion with the peripheral portions, are significantly lower than the stresses at the ends of a conventional, homogeneously bonded, assembly. Such maxima could be even below the yield stress of the solder material (in the numerical example in Chapter 6 of the Ref.6 the stress reduction because if the application of this type of an inhomogeneous bond was as high as about 35%). If this happens, the low-cycle fatigue condition will be avoided, the elastic stresses and strains will occur, and, owing to that, the lifetime of the solder joints will be much longer. It is noteworthy that the above results were obtained using analytical modeling [19-32] and, in the majority of cases, confirmed by FEA. Future work should be focused therefore mostly on experimental investigations and, particularly, on accelerated failure-oriented accelerated testing (FOAT) [33-37], to compare, for different package designs, the performances and lifetimes of conventional, homogeneous, and inhomogeneous designs.

Reference

1. E. Suhir, "Stresses in Bi Metal Thermost ats", ASME J. Appl. Mech., vol. 53, No. 3, Sept. 1986.
2. E. Suhir, "Interfacial Stresses in Bi-Metal Thermostats", ASME J. Appl. Mech., vol. 56, No. 3, September 1989
3. E. Suhir, Structural Analysis in Microelec tronic and Fiber Optic Systems, Van Nostrand Reinhold, New York, 1991.
4. J.H.Lau, Thermal Stress and Strain in Microelectronics Packaging, Van Nostrand Reinhold, 1993
5. J.S.Hwang, Modern Solder Technology for Competitive Electronics Manufacturing, McGraw-Hill, 1996
6. E.Suhir, Avoiding Inelastic Strain in Solder Material of IC Devices, CRC Press, 2020
7. E. Suhir, "Thermal Stress in a Bi-Material Assembly Adhesively Bonded at the Ends", J. Appl. Physics, vol. 89, No.1, 2001.
8. E.Suhir, "Design-for-Reliability and Accelerated-Testing of Solder Joint Interconnections", Chip Scale Reviews, Nov.-Dec. 2019
9. E.Suhir, "Interfacial Thermal Stresses in a Bi-Material Assembly with a Low-Yield-Stress Bonding Layer", Modeling and Simulation in Materials Science and Engineering, vol. 14, 2006
10. E. Suhir, "Predicted Stresses in a Ball-Grid-Array (BGA)/Column-Grid-Array (CGA) Assembly with a Low Modulus Solder at Its Ends", Journal of Materials Science: Materials in Electronics, vol.26, No.12, 2015
11. E. Suhir, "Bi-Material Assembly with a Low-Modulus-and/or-Low-Fabrication-Temperature Bonding Material at Its Ends: Optimized Stress Relief", Journal of Materials Science: Materials in Electronics, vol.27, No.5, 2016
12. E. Suhir, R. Ghaffarian, "Predicted Stresses in a Ball-Grid-Array (BGA)/Column-Grid-Array (CGA) Assembly with Epoxy Adhesive at Its Ends", Journal of Materials Science: Materials in Electronics, vol.27, No.5, 2016
13. E.Suhir, "Avoiding Low-Cycle Fatigue in Solder Material Using Inhomogeneous Column-Grid-Array (CGA) Design", ChipScale Reviews, March-April 2016

14. E. Suhir, R. Ghaffarian, J. Nicolics, "Could Thermal Stresses in an Inhomogeneous BGA/CGA System be Predicted Using a Model for a Homogeneously Bonded Assembly?", Journal of Materials Science: Materials in Electronics, vol.27, No. 1, 2016
15. E. Suhir, "Expected Stress Relief in a Bi-Material Inhomogeneously Bonded Assembly with a Low-Modulus-and/or-Low-Fabrication-Temperature Bonding Material at the Ends", Journal of Materials Science: Materials in Electronics, vol.27, No.6, 2016
16. E. Suhir, "Bi-Material Assembly Adhesively Bonded at the Ends and Fabrication Method", US Patent #6,460, 753, 2002
17. E. Suhir, "Thermal Stress in an Adhesive ly Bonded Joint with a Low Modulus Adhesive Layer at the Ends", J. Appl. Phys., April 2003
18. E. Suhir, S. Yi and R. Ghaffarian, "How Many Peripheral Solder Joints in a Surface Mounted Design Experience Inelastic Strains?", Journal of Electronic Materials, v.46, No.3, 2017
19. E. Suhir, A. Shakouri, "Assembly Bonded at the Ends: Could Thinner and Longer Legs Result in a Lower Thermal Stress in a Thermoelectric Module (TEM) Design?", ASME J. Appl. Mech., vol.79, No.6, 2012
20. E.Suhir, "Analytical Thermal Stress Model for a Typical Flip-Chip Package Design", Journal of Materials Science: Materials in Electronics, vol.29, No.4, 2018
21. E. Suhir, "Solder Joints in Surface Mounted IC Assemblies: Relief in Stress and Warpage Owing to the Application of Elevated Stand-off Heights". J of Modern Applied Physics,2(1), 2018
22. E. Suhir, "Analytical Thermal Stress Modeling in Electronic and Photonic Systems", ASME App. Mech. Reviews, vol.62, No.4, 2009.
23. E. Suhir, "Thermal Stress Modeling in Microelectronics and Photonics Packaging, and the Application of the Probabilistic Approach: Review and Extension", IMAPS Int. J. Microcircuits and Electronic Packaging, vol.23, No.2, 2000
24. E. Suhir, "Thermal Stress Failures: Predictive Modeling Explains the Reliability Physics Behind Them", IMAPS Advanced Microelectronics, vol.38, No.4, July/August 2011
25. E. Suhir, "Analytical Modeling Enables to Explain Paradoxical Situations in the Behavior and Performance of Electronic Materials and Products: Review", Journal of Physical Mathematics 07(01) • Dec. 2015
26. E. Suhir, "Analysis of a Short Beam with Application to Solder Joints: Could Larger Stand-off Heights Relieve Stress?", European Journal of Applied Physics (EPJAP), vol. 71, 2015
27. E. Suhir, R. Ghaffarian, J. Nicolics, "Could Application of Column-Grid-Array Technology Result in Inelastic-Strain-Free State-of-Stress in Solder Material?", Journal of Materials Science: Materials in Electronics, vol.26, No.12, 2015
28. E. Suhir, "Analytical Modeling Occupies a Special Place in the Modeling Effort", Short Comm., J.Phys.Math., 7(1), 2016
29. E. Suhir, "Bi-Material Assembly Subjected to Thermal Stress: Propensity to Delamination Assessed Using Interfacial Compliance Model", Journal of Materials Science: Materials in Electronics, vol.27, No.7, 2016
30. E.Suhir, "Analytical Modeling Enables Explanation of Paradoxical Behaviors of Electronic and Optical Materials and Assemblies", Advances in Materials Research, vol.6, No.2, 2017

31. E.Suhir, S.Yi, J.S.Hwang, R. Ghaffarian, “Elevated Stand-Off Heights of Solder Joint Interconnections Can Result in Appreciable Stress and Warpage Relief”, IMAPS J. of Microelectronics and Electronic Packaging, vol. 16, No. 1, Jan. 2019
32. E.Suhir, “Analytical Thermal Stress Modeling in Electronics and Photonics Engineering: Application of the Concept of Interfacial Compliance”, Journal of Thermal Stresses, special issue dedicated to 90-th birthday of Prof Richard Hetnarski, 2019, published on line
33. E.Suhir, “The Role of Failure-Oriented-Accelerated-Testing (FOAT) for Field Functional IC Packages”, Circuits Assembly, July 01, 2013
34. E. Suhir, “Electronics Reliability Cannot Be Assured, if it is not Quantified”, Chip Scale Reviews, March-April, 2014
35. E.Suhir, “Avoiding Low-Cycle Fatigue in Solder Material Using Inhomogeneous Column-Grid-Array (CGA) Design”, ChipScale Reviews, March-April 2016
36. E. Suhir, “Relieving Stress in Flip-Chip Solder Joints”, Chip Scale Reviews, v.21, No.5, September-October, 2017
37. E.Suhir, “Design-for-Reliability and Accelerated-Testing of Solder Joint Interconnections”, Chip Scale Reviews, Nov.-Dec. 2019

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